REMARKS

Applicants respectfully request the Examiner's reconsideration of the present application.

Claims 1-33 are pending in the present application.

Claims 1-3, 5-8, 12-17, 19, 21-23, 25-27, and 29-31 are rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent No. 6,871,328 ("Fung").

Claims 4, 9-11, 18, 20, 24, 28, and 32-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1, 4, 12, 15, 17-19, 28, 30, and 31 have been amended.

Support for the amended claims, 1, 4, 12, 15, 17-19, 28, 30, and 31, and for all pending claims is found on pages 4-29 of the specification, Figures 1-17 of the drawings, and claims 1-33 as originally filed. No new matter has been added.

Applicants refer the Examiner to Figures 13, 16-17, and pages 4, and 17-29 of the specification for a few illustrative embodiments that support the claims.

Claims 1-3, 5-8, 12-17, 19, 21-23, 25-27, and 29-31 are rejected under 35 U.S.C. §102(e) as being unpatentable over Fung. With respect to claims 1, 12, and 25, the Examiner states in part that

> As to claims 1, 12 and 25, Fung et al. teach a method for implementing a user logic design in a programmable logic device (PLD) or implementing logic design memory in physical memory devices of a PLD using placing and routing tools (Fig. 1 & 6 and its description). The placing and routing tools (EDA tool) is shown in Fig. 1. The EDA tool determines a first location on the PLD to place a user defined logic region in response to user specified constraints for placement of the user defined logic region (the placement and routing tools map one of user defined logic regions 908, 910 and 912 into one of locations 902, 904 and 906 of target devices in PLD 900 according to user defined constraints). The placement and routing tools also place said one of user defined logic regions 908, 910 and 912 into other one of locations 902, 904 and 906 of target devices in PLD 900 when it is applicable according to other user defined constraints (independent of the user defined constraints for placement) (Fig. 9).

(1/11/2006 Office Action, pp. 2-3).

It is submitted that Fung does not render claims 1-3, 5-8, 12-17, 19, 21-23, 25-27, and 29-31, as amended, unpatentable under 35 U.S.C. §102(e).

Fung includes a disclosure of a method for mapping logic design memory into physical memory devices of a programmable logic device. User constraints and physical constraints may be taken into account in generating the mapping solution. Functional block layout on the programmable logic device may be taken into account when generating the mapping solution. Multiple types of physical memory types may be considered and logic design memory may be mapped to those types of physical memory devices that are determined to be the most appropriate. A mapping solution may be optimized using, for example, simulated annealing. (Fung Abstract).

It is submitted that Fung does not teach or suggest a method for designing a system on a target device utilizing PLDs that includes determining a first location on the PLD to place a user defined logic region in response to user specified constraints for placement of the user defined logic region, and determining a second location to place the user defined logic region, wherein the second location is determined independent of the user specified constraints for placement.

On the contrary, Fung discloses a plurality of cliques 908, 910, and 912 from a constraint sub-group 914 and a plurality of physical memory devices 902, 904, and 906 on a programmable logic device 900 (col. 10, line 66 through col. 11, line 5). Applicants submit that the cliques 908, 910, and 912 are not user defined logic regions because they are not defined by a user. A clique is a plurality of memory slices that are grouped together by a logic design to hardware application, not a user (col. 10, lines 21-23). A logic design to hardware application is a design tool that may be implemented in software, hardware, or both (col. 4, lines 46-49).

In addition, the memory slices within clique 908, 910, and 912 are constrained to be placed within the same physical memory device (col. 10, lines 23-25). Applicants submit that a location to place the cliques 908, 910, and 912 are not determined in response to user specified constraints for placement. Cliques are placed onto physical memory based upon the size of a clique, and the size of the physical memory available not on user specified constraints for placement (col. 10, lines 56-66). For example, if clique 908 of size eight were the clique of largest size in constraint sub-group 914, then clique 908 may be mapped in three different locations (i.e., two different locations in physical memory device 902, and in physical memory device 904) (col. 11, lines 6-10).

Furthermore, Applicants submit that Fung does not teach or suggest both determining a first location for a user defined region in response to user specified constraints for placement and determining a second location for a user defined region independent of the user specified constraint for placement. Applicants submit that it is not clear from Figure 9 what the Examiner believes to be the first location determined for placement in response to user specified constraints for placement and the second location determined for placement independent of the user specified constraints.

In contrast, claim 1 as amended states

> A method for designing a system on a target device utilizing programmable logic device (PLD) with an electronic automation design tool (EDA), comprising:
> having the EDA tool determine a first location on the PLD to place a user defined logic region in response to user specified constraints for placement of the user defined logic region; and
> having the EDA tool determine a second location to place the user defined logic region, wherein the second location is determined independent of the user specified constraints for placement.

(Claim 1 as amended) (Emphasis added).

Claims 12, and 25, as amended, include similar limitations. Given that claims 2-11, 13-18, and 26-33, depend directly or indirectly from claims 1, 12, and 25, as

amended, it is likewise submitted that claims 2-11, 13-18, and 26-23 are also patentable under 35 U.S.C. §102(e) over Fung.

It is submitted that Fung does not teach or suggest a method for designing a system on a target device utilizing a PLD that includes determining whether the user specified constraint for placement is a soft constraint in response to the system not satisfying timing, and determining a second location to place the user defined logic region, wherein the second location is determined independent of the user specified constraints for placement if the user specified constraint is a soft constraint.

On the contrary, Fung does not disclose the use of soft constraints and the determination of a second location independent of the user specified constraint for placement if the user specified constraint is a soft constraint. Applicants respectfully request that the Examiner point out where it is believed that Fung makes this disclosure.

In contrast, claim 12 as amended states

> A method for positioning components of a system onto a target device utilizing a programmable logic devices (PLDs) using an electronic design automation tool, comprising:
> having the EDA tool determine a first location on the PLD to place a user defined logic region in response to user specified constraints for placement of the user defined logic region;
> determining whether the user specified constraint is a soft constraint in response to the system not satisfying timing; and
> having the EDA tool determine a second location to place the user defined logic region, wherein the second location is determined independent of the user specified constraints for placement if the user specified constraint is a soft constraint.

(Claim 12) (Emphasis added).

Given that claims 13-18 depend directly or indirectly from claim 12 as amended, it is likewise submitted that claims 13-18 are also patentable under 35 U.S.C. §102(e) over Fung.

It is submitted that Fung does not disclose determining routing strategies for routing signals on PLDs in response to user specified routing constraints, and

determining additional routing strategies for routing the signals independent of the user specified routing constraints, wherein the routing constraints pertain to a category of routing resources on the PLDs to use.

The Examiner cites column 5, lines 42-58 that references "any other suitable constraint" as evidence that Fung discloses user specified routing constraints (1/11/06 Office Action, p. 4). Applicants respectfully request that the Examiner point out where it is believed that Fung makes the disclosure of both determining routing strategies for routing signals in response to user specified routing constraints that pertain to categories of routing resources to use, and determining additional routing strategies for routing the signals where the additional routing strategies are independent of the user specified routing constraints.

In contrast, amended claim 19 states

> A method for designing a system on a programmable logic device (PLD) with an electronic design automation (EDA) tool, comprising:
> having the EDA tool determine routing strategies for routing signals on the PLD in response to user specified routing constraints that pertain to categories of routing resources to use; and
> having the EDA tool determine additional routing strategies for routing the signals on the PLD where the additional routing strategies are independent of the user specified routing constraints.

(Claim 19 as amended) (Emphasis added).

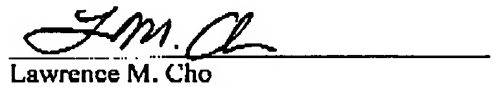
Given that claims 20-24, depend directly or indirectly from claim 19, as amended, it is likewise submitted that claims 20-24 are also patentable under 35 U.S.C. §102(e) over Fung.

In view of the amendments and arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-33, as amended, should be found to be in condition for allowance.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

Dated: April 10, 2006



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